

Description

PARTIAL WAFER BONDING AND DICING

BACKGROUND OF INVENTION

[0001] Field of the Invention

[0002] The invention presents a method of manufacturing integrated circuit chips that partially joins an integrated circuit wafer to a supporting wafer at a limited number of joining points.

[0003] Description of the Related Art

[0004] Within this application several publications are referenced by arabic numerals within parentheses. Full citations for these, and other, publications may be found at the end of the specification immediately preceding the claims. The disclosures of all these publications in their entireties are hereby expressly incorporated by reference into the present application for the purposes of indicating the background of the present invention and illustrating the state of the art. The below-referenced U.S. Patents disclose embodiments that were satisfactory for the pur-

poses for which they were intended. The disclosures of the below-referenced prior U.S. Patents, in their entireties, are hereby expressly incorporated by reference into the present invention for purposes including, but not limited to, indicating the background of the present invention and illustrating the state of the art.

[0005] In 1965, Dr. Gordon Moore, then Director of Research and Development for Fairchild Semiconductor, made the observation that the number of transistor devices per integrated circuit had been doubling every couple of years since the creation of the first integrated circuits in the late 1950's and that he expected the trend to continue for the foreseeable future. This observation was dubbed "Moore's Law" by the trade press. Now almost 40 years later, despite numerous dire predictions of fundamental obstacles, unrelenting industry efforts towards every-increasing semiconductor density have effectively affirmed Dr. Moore's prophetic observation, and the trend is still expected to continue unabated for the foreseeable future. The process of reducing semiconductor device size to increase integrated circuit density is generally referred to as "scaling".

[0006] In fact, because of the scaling, silicon based process tech-

nologies have facilitated a tremendous increase in the frequency range of operation for both digital and analog circuits. The fast transistors combined with low defect densities open the door to integration of complex high-speed micro-electronic systems on a single chip, which was simply not feasible or economical before. Unfortunately, such ultra-high-frequency integrated systems mandate a paradigm shift in the packaging methodology and thermal managements. Conventional chip/module cooling schemes can no longer handle the thermal dissipation of this new generation of chips. A new cooling concept to effectively remove heat from the chip and module is urgently needed.

[0007] There are many motivations for thinning a die. The primary motivation is to improve the thermal conductivity. As wafer thickness is increased, thermal dissipation from the back side of the wafer presents a challenge. The situation is aggravated when a buried oxide layer is presented on a SOI (Silicon on Insulator) wafer which is used to enhance device performance.

[0008] On the other hand, in order to enable ultra high density 3-Dimensional stacked packaging of flash memory and SRAM IC for portable electronics, thin dies are necessary

to save space. To thin down a die, especially after a wafer's C4 solder balls or wire-bond pads are formed, wafer tested, diced, and picked is definitely not an easy task. In the past, a special set up to polish down the back side of the die with the front size fully protected is one of the conventional approaches. This method is not only expensive, but also results in potential reliability concerns, and is therefore not manufacturable.

[0009] One example of temporary bonding, called reversible bonding was proposed by et al. and titled "Reversible Wafer Bonding for Reliable Compound Processing". They suggested the use of wax or dry film adhesives to bond a wafer to a silicon carrier to enhance the mechanical strength during processing. The two substrates are separated after the processing is completed. Similar methods are used in US Patent 4,962,879 and US Patent 6,010,591 (incorporated herein by reference), both are methods to bond two wafers during transportation, handling and processing. They are separated after processing. Unfortunately, all the conventional reversible bonding methods are not suitable for high-temperature processing. During semiconductor processing, especially during steps such as diffusion, oxidation and annealing, the wafer substrate

must endure temperature as high as 1100°C . All the reversible bonding methods so far can only sustain a temperature limit of 150°C . Neither method is cost-effective or reliable. Both etching and mechanical polishing are time consuming. The chemicals used for etching and polishing are prone to attack circuits and C4 balls on the front side of the die. A good protective coating and secure holding to avoid damage is a challenge. Besides, neither method is able precisely stop at a predetermined thickness during the thinning process.

SUMMARY OF INVENTION

[0010] The invention presents a method of manufacturing integrated circuit chips that partially joins an integrated circuit wafer to a supporting wafer at a limited number of joining points. Once joined, the integrated circuit wafer is chemically-mechanically polished to reduce the thickness of the integrated circuit wafer. Then, after reducing the thickness of the integrated circuit wafer, the invention performs conventional processing on the integrated circuit wafer to form devices and wiring in and on the integrated circuit wafer. Next, the invention cuts through the integrated circuit wafer and the supporting wafer to form chip sections. During this cutting process, the integrated

circuit wafer separates from the supporting wafer in chip sections where the integrated circuit wafer is not joined to the supporting wafer by the joining points. Chip sections where the integrated circuit wafer remains joined to the supporting wafer are thicker than the chips sections where the integrated circuit wafer separates from the supporting wafer.

[0011] The invention aligns the integrated circuit wafer to the supporting wafer before joining the two. Also, before joining the integrated circuit wafer to the supporting wafer, the invention roughens portions of the integrated circuit wafer facing the supporting wafer to create rough surface portions on the integrated circuit wafer. This roughening process avoids producing rough surface portions adjacent the joining points.

[0012] The joining process comprises a bonding process, such as a thermal oxide bonding process. This creates high-temperature joining points that can survive processing temperatures that are reached during the processing that forms the devices and the wiring in the integrated circuit wafer.

[0013] These, and other, aspects and objects of the present invention will be better appreciated and understood when

considered in conjunction with the following description and the accompanying drawings. It should be understood, however, that the following description, while indicating preferred embodiments of the present invention and numerous specific details thereof, is given by way of illustration and not of limitation. Many changes and modifications may be made within the scope of the present invention without departing from the spirit thereof, and the invention includes all such modifications.

BRIEF DESCRIPTION OF DRAWINGS

- [0014] The invention will be better understood from the following detailed description with reference to the drawings, in which:
- [0015] Figure 1 is a schematic diagram of a partially completed supporting wafer according to the invention;
- [0016] Figure 2 is a schematic diagram of a partially completed supporting wafer according to the invention;
- [0017] Figure 3 is a schematic diagram of a partially completed supporting wafer according to the invention;
- [0018] Figure 4 is a schematic diagram of a partially completed supporting wafer according to the invention;
- [0019] Figure 5 is a schematic diagram of a partially completed supporting wafer according to the invention;

- [0020] Figure 6 is a schematic diagram of a partially completed supporting wafer according to the invention;
- [0021] Figure 7 is a schematic diagram of a partially completed supporting wafer according to the invention;
- [0022] Figure 8 is a schematic diagram of an integrated circuit wafer and supporting wafer according to the invention;
- [0023] Figure 9 is a schematic diagram of an integrated circuit wafer and supporting wafer according to the invention;
- [0024] Figure 10 is a schematic diagram of an integrated circuit wafer and supporting wafer according to the invention;
- [0025] Figure 11 is a schematic diagram of an integrated circuit wafer and supporting wafer according to the invention;
- [0026] Figure 12 is a schematic diagram of an integrated circuit wafer and supporting wafer according to the invention;
- [0027] Figure 13 is a schematic diagram of an integrated circuit wafer and supporting wafer according to the invention;
- [0028] Figure 14 is a schematic diagram of an integrated circuit wafer and supporting wafer according to the invention;
- [0029] Figure 15 is a schematic top-view diagram of an integrated circuit wafer and joining areas; and
- [0030] Figure 16 is a flow diagram illustrating a preferred method of the invention.

DETAILED DESCRIPTION

[0031] The present invention and the various features and advantageous details thereof are explained more fully with reference to the nonlimiting embodiments that are illustrated in the accompanying drawings and detailed in the following description. It should be noted that the features illustrated in the drawings are not necessarily drawn to scale. Descriptions of well-known components and processing techniques are omitted so as to not unnecessarily obscure the present invention. The examples used herein are intended merely to facilitate an understanding of ways in which the invention may be practiced and to further enable those of skill in the art to practice the invention. Accordingly, the examples should not be construed as limiting the scope of the invention.

[0032] As discussed above, one motivation of wafer thinning is to improve the thermal conductivity. Also, in order to enable ultra high density 3-Dimensional stacked packaging of flash memory and SRAM IC for portable electronics, thin dies are necessary to save space. Another reason for thinning wafers is to prepare a failing module for a) analytical optical measurement (with IR, InfraRed) of the front-side circuit operation through the backside (e.g., PICA, Emission Microscopy); b) preparation for backside Focused Ion

Beam (FIB) circuit editing during design debug; or c) removal of the majority of the silicon for later wet etching to reveal gate oxide defects. In all of these cases, the endpoint is primarily mechanical from the polishing apparatus. With conventional techniques, the technician's skill is a critical asset here, one needs to have a good "feel" for how various parts polish. There are ways to take a part off the polishing machine and measure optically, but this is tedious at best and destructive of samples due to repeated mounting and dismounting in the worst case. The conventional throughput is pretty poor for a manufacturing process, about 1 – 3 hours per module, but is perfectly acceptable for Failure Analysis.

[0033] Dry (and wet) etching were considered as potential solutions to the problems shown above. Unfortunately, an optical finish is required to see through the chip with little distortion, and all etched surfaces have not been smooth enough for this purpose. While the surface could be polished, for Failure Analysis application with the conventional processing: 1) the etch is not significantly faster, 2) the protective coating application adds setup time, 3) the protective coating needs to be removed for polishing, 4) establishing planarity between the sample and the polish-

ing platen requires actual polishing, observation, and mechanical measurement of the progress and the mechanical measurements cannot be carried out below about 200 microns, 5) the polishing tool (manual) costs less than the etching tool, and 6) etching requires more floor space and environmental protection support equipment.

[0034] In order to address these concerns, the invention thins the die by using a "partial wafer bonding" technique. With this technique, bonding applies only to wafer edges and/or some selected chip areas. In other words, partial bonding only bonds the areas where no thinning is required. These areas include test sites, end-point sites, the dummy fillers, etc. The concept can be extended to use such partial bonding techniques to create a mixture of thin and thick dies after dicing. Figures 1-7 illustrate different ways of forming the support wafer, and Figures 8-12 illustrate how the invention bonds and separates the integrated circuit wafer to and from the support wafer.

[0035] More specifically, Figure 1 illustrates a substrate 12 (such as a silicon substrate) with an overlying oxide layer 10 formed using any conventional oxidation technique. In Figure 2, a nitride layer 20 is deposited over the oxide layer 10 and a mask 22 (such as any conventional pho-

toresist mask) is patterned over the nitride 20. Next, as shown in Figure 3, the nitride 20 and oxide 10 are patterned through the mask 22 using single, or multiple etching processes (or other similar material removal processes) and the mask 22 is similarly removed. Then, in Figure 4, additional oxide 40 is formed/grown to produce a support wafer that has an upper surface of nitride regions 20 and oxide regions 40. The structure shown in Figure 4 can then be used in the subsequent processing shown in Figures 8–14.

[0036] Figures 5–7 illustrate a different method for forming the support wafer. Rather than stopping the etching process on the substrate 12 as shown in Figure 3, in this embodiment, the etching processes continues to etch a portion of the substrate away, as shown Figure 5. Before or after this, the mask 22 (shown in Figure 2) can be removed. Then, the additional oxide 40 is formed as shown in Figure 6. Next, the structure is planarized, as shown Figure 7, such that it includes regions of oxide 40 along the smooth upper surface of silicon substrate 12.

[0037] As shown in Figures 8–12, the invention presents a method of manufacturing integrated circuit chips that partially joins an integrated circuit wafer 84 to a support–

ing wafer 80 at a limited number of joining points 88. Two similarly sized wafers 80, 84 with similar or different thickness are used for bonding. In this example, the top wafer 84 can be a good quality wafer having a much thinner thickness (1/2 the thickness or less) than the bottom holding wafer 80.

[0038] The joining process is represented by the double arrow in Figure 8, which results in the structure shown Figure 9, and comprises a bonding process, such as a thermal oxide bonding process. This joins the two wafers 80, 84 only at the high-temperature joining points 88 (shown only in Figure 8 for clarity). These joining points 88 can survive processing temperatures of 850–1200 °C that are reached during the processing that forms the devices and the wiring 110 (shown in Figure 11) in the integrated circuit wafer 84. The bonding agent, such as a grown thermal oxide layer 82 is patterned on the support wafer on specific areas where bonding is desirable using, for example, the processing shown in Figures 1–7.

[0039] The invention aligns the integrated circuit wafer 84 to the supporting wafer 80 before joining the two. Also, before joining the integrated circuit wafer 84 to the supporting wafer 80, the invention can roughen (or recessed back by

20 to 50 nm to avoid physical contact during bonding) the portions of the integrated circuit wafer 84 facing the supporting wafer 80 in areas that will not be joined to the adjacent wafer to create rough surface portions 86 on the integrated circuit wafer 84. The roughening process can comprise chemical etching, reactive ion etching, depositing black silicon while the smooth areas are coated, etc.

[0040] This roughening process avoids producing rough surface portions 86 adjacent the joining points 88. A bonding surface should be optically smooth or mirror-like surface in order to have a good quality of bonding. Therefore, joining points 88 have an optically smooth surface.

[0041] Therefore, as shown in Figure 8, the areas that will avoid bonding 86 can alternatively have an interface with some trapped nitrogen 20. Therefore, item 86 in the drawings alternatively represents an area that includes nitrogen in sufficient quantity to prevent wafer bonding (this area can also be roughened). The nitride regions 20, or nitrogen rich film 20, during the bonding process would produce an outgassing of nitrogen to prevent the two surfaces from bonding together.

[0042] During wafer bonding, as shown in Figures 8 and 9, the two wafers are contacted to each other in a reactor and

heated to a temperature range of 850 to 1200 °C in a suitable ambient. After bonding, only the joining points 88 defined by bonding agent 82 will be glued together.

[0043] Once joined, the integrated circuit wafer 84 is chemically-mechanically polished to reduce the thickness of the integrated circuit wafer 84, as shown in Figure 10 where the dashed line 100 shows the pre-polishing thickness. Then, after reducing the thickness of the integrated circuit wafer 84, the invention performs conventional processing on the integrated circuit wafer 84 to form devices 110 and wiring 114 in and on the integrated circuit wafer 84, as shown in Figure 11. Once the devices and circuits 110 are formed, terminal metals are patterned and C4 solder ball connections 112 are formed, and the wafer is tested.

[0044] Next, as shown by the dashed vertical lines 120 in Figure 12, the invention cuts through the integrated circuit wafer 84 and the supporting wafer 80 to form chip sections 122, 124. During this cutting process, the integrated circuit wafer 84 separates from the supporting wafer 80 in chip sections 124 where the integrated circuit wafer 84 is not joined to the supporting wafer 80 by the joining points 88 (e.g., where regions 86 prevents the wafers from joining). Chip sections 122 do not separate during

the cutting process. Therefore, chip sections 122 where the wafer 84 remains joined to the supporting wafer 80 are thicker than the chips sections 124 where the integrated circuit wafer 84 separates from the supporting wafer 80.

[0045] In this dicing process shown in Figure 12, both the top and bottom surfaces can be protected by adhesive films 126 to protect the dies, especially for very thin dies. These thin chips can be etched out by etching through the thin top silicon layer 84 and the thin dies can all be attached from the top layer since they are not bonded to the surface wafer 80.

[0046] Once the wafer is cut, both thin 124 and thick dies 122 are produced. The thick dies may be scrapped or used for other purposes such as test sites, end point sites, dummy fillers, etc. After dicing, the thin dices 124 have a very thin substrate thickness, but also due to its rough back surface 86, the thermal conductivity of the thin dies 124 is greatly improved.

[0047] Figures 13 and 14 show partial dicing, where the chips are individually diced. In this process, the wafer is only cut to the level of the supporting wafer 80. This allows the integrated circuit sections 124 that are not jointed to the sup-

porting wafer to release from the supporting wafer 80, while the other chip sections 122 remain attached to the supporting wafer 80. These thin chips 124 which are not bonded to the carrier wafer 80 can be etched out by etching through the thin top silicon layer 84 and the thin dies 124 can all be detached from the top.

[0048] The cutting can also be done by using laser, ion beam or other means. The thin coating 122 of, for example, an organic protective layer can be dissolved in a solvent after dicing. Dicing can be done by using laser cutting techniques especially on those thin dies. For testing purposes, one can pick one good thin die for laser cutting and send this selected die ahead for module mounting. This provides flexibility in manufacturing.

[0049] As shown in Figure 15, the invention bonds only some limited predetermined areas so to allow better manufacturability. More specifically, Figure 15 represents a top view of a wafer (e.g., 80) and the darkened areas 140 are the only areas of the wafer that will be bonded to the adjacent wafer (e.g., 84). As shown in this example, the bonding area 140 is only on the edge of the wafer, and at selected areas 140 that do not require thinning (or that can be scrapped). The bonding pattern is designed based

on the existing chip layout which will be patterned on the integrated circuit wafer 84. After bonding, the wafer will have the proper thickness for handling and processing. The edges of the wafers are preferably bonded and sealed so that no chemical will get through the interface of two wafers and so that there is no possibility of detaching under the full course of chip processing environments. Thus, the bonded areas can be along the perimeter of wafer (e.g., a ring-shape 5mm width bonding zone) and another 5 to 10 selected dies (uniformly distributed, taking yield loss after dicing).

[0050] Figure 16 shows the processing of the invention in flowchart form. More specifically, in item 160, the invention partially joins an integrated circuit wafer to a supporting wafer at a limited number of joining points. Once joined, the integrated circuit wafer is chemically-mechanically polished 162 to reduce the thickness of the integrated circuit wafer. Then, after reducing the thickness of the integrated circuit wafer, the invention performs conventional processing on the integrated circuit wafer to form devices and wiring 164 in the integrated circuit wafer. Next, the invention cuts through the integrated circuit wafer and the supporting wafer 166 to form chip sec-

tions. During this cutting process, the integrated circuit wafer separates from the supporting wafer in chip sections where the integrated circuit wafer is not joined to the supporting wafer by the joining points. Chip sections where the integrated circuit wafer remains joined to the supporting wafer are thicker than the chips sections where the integrated circuit wafer separates from the supporting wafer.

[0051] The invention presents a number of advantages when compared to conventional wafer thinning processes. First, because the supporting wafer 80 supports the integrated circuit wafer 84 during processing, the thickness of the integrated circuit wafer 84 can be reduced substantially when compared to conventional thin wafers. Further, because the invention thins the wafer before the devices, wiring, and interconnects 110 are formed, the invention increases yield by reducing any damage to such devices 110. Also, because the invention uses a high temperature bond 82, the invention maintains contact between the supporting wafer 80 and the integrated circuit wafer 84 during most of the high-temperature processing, again, increasing yield. Additionally, the invention can use a chemical-mechanical polishing process which allows sub-

stantial improvements in control of how much the thickness of the wafer can be reduced, especially when compared to conventional dry and wet etching processes.

[0052] While the invention has been described in terms of preferred embodiments, those skilled in the art will recognize that the invention can be practiced with modification within the spirit and scope of the appended claims.